

LISTING OF THE CLAIMS:

1-41. (Canceled)

42.(New) A non-volatile semiconductor memory device, comprising:

a memory array including a plurality of multi-level-cell memory cells, each memory cell comprising a storage element having a capacity to store N bits of logical data,

where  $N \geq 2$ , and each memory cell configured for  $2^N$  distinct data storage levels, each of the  $2^N$  data storage levels representative of a discrete N-bit combination of logical data; and

a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells and inhibiting programming of a memory cell programmed to substantially within a selected data storage level.

43.(New) The device of claim 42, wherein the storage element comprises a semiconductor transistor having a programmable threshold voltage,  $V_t$ , within a continuous range from a lowest  $V_t$  value to a highest  $V_t$  value, the continuous range having  $2^N$  distinct data storage levels including an erased level and  $2^N-1$  program levels, the  $2^N-1$  program levels including a lowest program level, at least one intermediate program level, and a highest program level.